IN THE CLAIMS

1. (Currently Amended) An etching method comprising:

providing a wafer having a dielectric layer and plurality of electrodes separated from each other;

planarizing the electrodes and the dielectric layer such that top surfaces of the electrodes are coplanar with the top surface of the dielectric layer;

after planarizing the electrodes and the dielectric layer, wet etching the wafer including the dielectric layer and separated electrodes such that at least one of the electrodes partially protrudes from the top surface of the dielectric layer;

~~providing a wafer having a dielectric layer and a plurality of electrodes separated from each other, wherein at least one of the plurality of electrodes partially protrudes from a top surface of the dielectric layer;~~

etching the dielectric layer with a chemical solution; and

prior to etching the dielectric layer, reducing the protruding portion of the electrode, wherein reducing the protruding portion includes recessing a top surface of the electrode at least 500 angstroms below the top surface of the dielectric layer.

2. (Original) The method of claim 1, wherein the protruding portion of the electrode is reduced sufficiently to prevent any bubbles included in the chemical solution from adhering to the electrode.

3-6. (Canceled)

7. (Original) The method of claim 1, wherein reducing the protruding portion comprises dry etching.

8. (Original) The method of claim 7, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2 and combinations thereof.

9. (Original) The method of claim 1, wherein reducing the protruding portion comprises wet etching.

10. (Original) The method of claim 9, wherein wet etching uses a polysilicon etchant.

11-41. (Canceled)

42. (Previously presented) The method of claim 1, wherein the dielectric layer includes an oxide.

43. (Currently Amended) A method of preventing bubbles from adhering to a substantially cylindrical electrode having a sidewall portion and a bottom portion during a dielectric layer etching process, the method comprising:

providing a semiconductor substrate having the substantially cylindrical electrode, a first dielectric layer, and a second dielectric layer formed over the substrate, where the first dielectric layer surrounds the sidewall portion of the electrode and the second dielectric layer is formed in between the sidewall portion to cover the bottom portion of the electrode, and where an upper portion of the sidewall portion of the electrode protrudes above top surfaces of the first and second dielectric layers;

etching the electrode to recess the upper portion of the electrode below the top surfaces of the first and second dielectric layers; and

thereafter, etching the first and second dielectric layers in the dielectric layer etching process to expose substantially all of the sidewall portion of the electrode.

44. (Previously presented) The method of claim 43, wherein the upper electrode is etched below the top surfaces of the first and second dielectric layers such that a recession having a width substantially equal to the width of the sidewall portion of the electrode is formed between the first and second dielectric layers.

45. (Previously presented) The method of claim 43, wherein the top surface of the first dielectric layer is located at substantially the same height above the substrate as the top surface of the second dielectric layer.

46. (Previously presented) The method claim 43, wherein the first and second dielectric layers include an oxide.

47. (Currently Amended) An etching method comprising:

providing a wafer having a an electrode and a dielectric layer, where the dielectric layer is formed over a top surface of the electrode;

planarizing the electrode and dielectric layer such that a top surface of the dielectric layer is ~~substantially~~ coplanar with the top surface of the electrode;

wet cleaning the top surfaces of the electrode and dielectric layer such that the top surface of the electrode protrudes from the top surface of the dielectric layer;

etching the dielectric layer with a chemical solution; and

prior to etching the dielectric layer, reducing the protruding portion of the electrode, wherein reducing the protruding portion includes recessing a top surface of the electrode below the top surface of the dielectric layer.

48. (Currently Amended) An etching method comprising:

providing a wafer having a dielectric layer and an electrode including sidewalls having inner and outer surfaces, wherein a portion of the sidewalls partially ~~protrude~~ protrudes from a top surface of the dielectric layer such that the inner and outer surfaces of the protruding portion of the sidewalls are exposed;

etching the dielectric layer with a chemical solution; and

prior to etching the dielectric layer, reducing the protruding portion of the electrode, wherein reducing the protruding portion includes recessing a top surface of the electrode below the top surface of the dielectric layer.

49. (Canceled)

50. (New) The method of claim 43, wherein etching the electrode comprises dry etching.

51. (New) The method of claim 50, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2 and combinations thereof.

52. (New) The method of claim 43, wherein etching the electrode comprises wet etching.

53. (New) The method of claim 52, wherein wet etching uses a polysilicon etchant.

54. (New) The method of claim 48, wherein etching the electrode comprises dry etching.

55. (New) The method of claim 54, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2 and combinations thereof.

56. (New) The method of claim 48, wherein etching the electrode comprises wet etching.

57. (New) The method of claim 56, wherein wet etching uses a polysilicon etchant.

58. (New) The method of claim 48, wherein the dielectric layer includes an oxide.